MASTER IN SCIENCES AND TECHNOLOGY

EMBEDDED ELECTRONIC SYSTEMS

COURSE OUTLINE AND GUIDELINES

Academic Year 2015–2016
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COURSE STRUCTURE

The Master’s Programme comprises:

For students with a 4-year Bachelor’s Degree minimum and with a specialisation in Electronic/Instrumentation/Electrical Engineering/Automation:
Sem 2 – Academic (on campus)
Sem 3 – Academic (on campus)
Sem 4 – Internship (company/laboratory)

For students with a 3-year Bachelor’s degree OR with a 4-year Bachelor’s Degree in another engineering stream:
Sem 1 – Academic (on campus)
Sem 2 – Academic (on campus)
Sem 3 – Academic (on campus)
Sem 4 – Internship (company/laboratory)

The first three academic semesters* are offered between September 2014 and January 2016. Lectures, tutorials, lab work, practical work, projects, conferences and/or seminars make up the academic semesters. Evaluation, in the form of tests, quizzes, exams, etc. is conducted on a regular basis. Faculty members are from ESIGELEC as well as partner companies and universities, from France or abroad.

* (2 semesters in the case of students granted direct entry into the second semester, beginning February 2015)

The final semester is devoted to industrial/research experience, during which students must do a mandatory internship in a company or laboratory for a period of 4 months (min.) to 6 months (max.). While ESIGELEC provides assistance to find the internships, students are expected to play an active part, as ESIGELEC does not hand them out automatically. The students have up to a maximum of two years, after the final academic semester:

- to find and complete the internship
- to submit a professional thesis and make an oral presentation before a convened jury

Failure to meet these requirements may result in the degree not being awarded.

The Student Status

Registered Student status & Enrolled Student status

The final semester comprises three stages, i.e. completing the internship, submitting the professional thesis and the oral presentation before a jury convened by ESIGELEC.

Students are considered Registered Students of ESIGELEC for a period of 6 months after the end of the last academic semester. During this time, students are expected to complete the three aforesaid stages. The Registered Student status will be extended if a student has started the internship but has not completed second/third stage. The Registered Student status will cease to apply in the event that a student completes the oral presentation prior to the stipulated period of 6 months.

In the case of students not starting the internship in the six months following the end of the final academic semester, they will have to re-enrol and will be considered Enrolled Students of ESIGELEC.
The Registered Student status will take effect again upon commencement of the internship and remain valid until such time the student has completed all three stages therein involved.

A student has a maximum period of two years to complete the three stages of the internship semester. The students’ personal insurance must be valid for this entire period.

*Also refer Internship section.*

**PROGRAMME OBJECTIVES**

The Master’s Programme seeks to equip the students with the relevant knowledge, professional skills and practical experience in Electronics and Embedded Systems for industry or for research. They will learn how to design, develop and implement information in different sectors. Students will also acquire basic managerial skills.

The international environment at ESIGELEC allows students to discover new cultures and languages. Students must appear for the DELF certification exams in French (or TOEIC for French speaking students). The mandatory internship gives the students a hands-on experience in the work environment. Our graduates find job opportunities as developers, project managers, consultants or researchers in the field of information systems.

**ATTENDANCE POLICY**

ESIGELEC views class attendance as the student’s individual responsibility. Students are expected to comply with ESIGELEC’s attendance policy throughout their study period. All lectures, tutorials, practical work, projects, conferences and seminars are mandatory. Attendance will be monitored by the faculty members at the beginning of each class and the attendance sheet will be maintained by the Studies Office of ESIGELEC.

**Late entry into class:**
If a student is late by 10 or more minutes, he/she will be refused entry into the classroom and the faculty member will make a note in the attendance register.

**Absence from class:**
A student who is absent for medical reasons must submit a medical certificate within 3 working days, in order for the absence to be excused.

Leave letters in the case of other accepted anticipated absences must be signed at least 8 days prior to the absence, by the Academic Coordinator of the Master’s Programme, in order for the absence to be excused.

No other justifications of absence will be excused by ESIGELEC.
Penalty

Students will receive an oral warning after 5 occurrences (late entry or unjustified absence). A stern oral warning will be given after 10 instances. 20 such cases may lead to the student’s dismissal from ESIGELEC.

Absence from examination:
• only students whose absence from an examination has been justified will be allowed to re-take an examination.
• students whose absence from an examination has not been justified will be marked 0/20 in the said examination.

EVALUATION

Evaluation may include tests, quizzes, presentations or other formats as decided by the faculty members, who may also authorise the use of reference documents or calculators, if they deem it necessary. Each such test will be graded on a maximum mark of 20.

Scores & ECTS (European Credit Transfer System)
• The Master’s Programme is divided into several weighted courses, all of which include one or more weighted modules. Each course represents a certain number of credits.
• The score of a module is the average of the weighted scores of the different evaluation processes conducted within the same module.
• The score of a course is the result of the weighted averages of all modules of the course.
• The final overall score of the student is the result of the weighted averages of all courses of the Master’s Programme.
• The total number of ECTS of the Master’s Programme is equal to the total of all the ECTS of its courses.
• One ECTS corresponds to about 25 hours of course work (lectures, projects, practical work, evaluation, individual work).
• Students who are granted entry directly to the second semester, beginning September 2015, will automatically be awarded 30 ECTS, equivalent to the first semester of the Master’s Programme.
• A statement of marks is sent to the students at the end of each academic semester and also after they are presented at the Jury of ESIGELEC.

FRAUD AND CHEATING

Students indulging in fraudulent practices/ cheating during an exam/ oral presentation/ project/ practical work will be marked 0/20.
Examples of plagiarism, fraud or cheating, include, but are not limited to:
• Duplication of another student’s work during a written assignment / exam;
• Use of a reference document or calculator not authorized by the faculty member;
• Plagiarism (>20%) of reports, presentation, or computing programs, obtained by any means (book, magazine, other students, electronic files, Internet, work previously submitted in another course).
AWARDING THE MASTER’S DEGREE

Each academic semester at ESIGELEC carries a total of 30 ECTS. The internship, professional thesis and professional presentation also carry a total of 30 ECTS. A student must obtain a minimum score of 10/20 in each course to be awarded the allocated ECTS.

The Master’s Degree is awarded if the student has obtained a minimum of 10/20 in all courses, thereby obtaining the total number of 120 credits.

The jury of ESIGELEC for the Master’s Degree comprises the President, the Academic Coordinator of the Master’s Programme, and faculty members, and representatives of the managing staff of the school. This jury is chosen by the General Director of ESIGELEC, convenes up to a maximum of four times per year (April, July, September and December).

If students do not obtain the requisite number of ECTS to be awarded the Master’s Degree, even after re-taking exams, they will only receive an attestation from ESIGELEC mentioning the total number of ECTS obtained in the different courses. The total number of ECTS will be the total of the ECTS of the courses in which the students have obtained a minimum average score of 10/20.

The Master in Sciences and Technology, with specialisation in Electronic Embedded Systems, awarded by ESIGELEC to the graduated students is accredited by the French Ministry of Higher Education and Research.

RETYING EXAMS

If a student has obtained less than 10/20 in one or more courses in the academic semesters at ESIGELEC, the student will be asked to retake one or more exams in one or more modules of the courses concerned, as advised by the Academic Coordinator of the Master’s Programme (even if the final overall score of the student in the Master’s Programme is greater than 10/20).

If a student does not obtain the 30 ECTS in the final semester (internship), the Academic Coordinator of the Master’s Programme may:

• Instruct the student to redo a new internship, including submission of a professional thesis and an oral presentation, or;
• Instruct the student to submit a fresh report and/or redo the oral presentation, or;
• Deny the award of 30 ECTS, on the grounds of misconduct during the internship.

The scores obtained from exams retaken replace the previous scores obtained by the student in the modules concerned and a new average score will be calculated for the course(s) concerned.

If the student does not retake an exam as advised by the Academic Coordinator, the student will be marked 0/20 for the module.

The new average of the courses must be greater than 10/20 in order to obtain the requisite credits.
## Modules and Credits

<table>
<thead>
<tr>
<th>SEMESTER</th>
<th>CREDITS</th>
<th>MODULES &amp; COURSES</th>
<th>HOURS</th>
<th>WEIGHT</th>
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<tbody>
<tr>
<td><strong>SEM 1 (270 h)</strong>&lt;br&gt;From September 2014 to January 2015</td>
<td>6</td>
<td><strong>Electrical Engineering</strong>&lt;br&gt;MSTSEE11: Binary Logic and Digital Functions</td>
<td>30 h</td>
<td>4</td>
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<tr>
<td></td>
<td></td>
<td>MSTSEE12: Automatic</td>
<td>20 h</td>
<td>2</td>
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<tr>
<td></td>
<td>8</td>
<td><strong>Computer Science</strong>&lt;br&gt;MSTSEE13: Object Oriented Programming with Java</td>
<td>40 h</td>
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<td>MSTSEE14: C Programming</td>
<td>30 h</td>
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<td>6</td>
<td><strong>Project</strong>&lt;br&gt;MSTSEE15: Minor Project</td>
<td>60 h</td>
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<td>5</td>
<td><strong>Electronic</strong>&lt;br&gt;MSTSEE16: Fundamentals of Electronics</td>
<td>30 h</td>
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<td></td>
<td>5</td>
<td><strong>Foreign Languages</strong>&lt;br&gt;MSTENG: English as a Foreign Language or MSTFRE: French as a Foreign Language</td>
<td>60 h</td>
<td>5</td>
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<tr>
<td><strong>SEM 2 (364 h)</strong>&lt;br&gt;From February 2015 to July 2015</td>
<td>8</td>
<td><strong>Digital Systems</strong>&lt;br&gt;MSTSEE21: Microprocessors</td>
<td>62 h</td>
<td>4</td>
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<tr>
<td></td>
<td></td>
<td>MSTSEE22: VHDL and Logic Synthesis</td>
<td>40 h</td>
<td>3</td>
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<td></td>
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<td>MSTSEE23: Communication Busses</td>
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<td></td>
<td>12</td>
<td><strong>Embedded Software</strong>&lt;br&gt;MSTSEE24: Real-Time Operating Systems</td>
<td>40 h</td>
<td>3</td>
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<td>MSTSEE25: Embedded Linux</td>
<td>30 h</td>
<td>3</td>
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<td>MSTSEE26: Embedded C Programming</td>
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<td>3</td>
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<td></td>
<td></td>
<td>MSTSEE27: Embedded Java</td>
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<td><strong>Instrumentation</strong>&lt;br&gt;MSTSEE28: Virtual Instrumentation</td>
<td>30 h</td>
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<td>MSTSEE29: Specific Instrumentation</td>
<td>30 h</td>
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<td>4</td>
<td><strong>Language</strong>&lt;br&gt;MSTFRE: French as a Foreign Language or MSTENG: English as a Foreign Language</td>
<td>32 h</td>
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<td><strong>SEM 3 (326 h)</strong>&lt;br&gt;From September 2015 to January 2016</td>
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<td><strong>Embedded Communication</strong>&lt;br&gt;MSTSEE31: MtoM Communication</td>
<td>30 h</td>
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<td>MSTSEE32: Smart Sensors</td>
<td>20 h</td>
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<td>8</td>
<td><strong>Embedded Electronics</strong>&lt;br&gt;MSTSEE33: System on Chip</td>
<td>20 h</td>
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<td>MSTSEE34: DSP Processors</td>
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<td>MSTSEE35: Safety Systems</td>
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<td>8</td>
<td><strong>Course: Management and Language</strong>&lt;br&gt;MSTSEE36/37: Cross Cultural Awareness/Teamworking</td>
<td>36 h</td>
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<td></td>
<td>MSTSEE38: Oral Communication</td>
<td>14 h</td>
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<td></td>
<td>MSTSEEFRE: French as a Foreign Language or MSTSEEENG: English as a Foreign Language</td>
<td>30 h + 30 h</td>
<td>4</td>
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<td></td>
<td>8</td>
<td><strong>Course: Technical Projects</strong>&lt;br&gt;MSTSEE39: Project Management</td>
<td>26 h</td>
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<td>MSTSEE3A: Engineering Project</td>
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<td>MSTSEE41: INTERNSHIP of 4 to 6 months</td>
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<tr>
<td><strong>SEM 4</strong>&lt;br&gt;From February 2016</td>
<td>30</td>
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</table>
COURSE CURRICULUM AND SYLLABUS

Course title
Binary Logic and Digital Functions

Objectives
At the end of this course, students will be able to:
• to analyse and design digital functions

List of topics
• Number representation
• Fundamentals of Boolean algebra
• Construction of elementary gates
• Circuits developed from combinatory logic (comparator, decoder and demultiplexer)
• Introduction to sequential logic and its basic components (D, RS, RSH, and JK flip flops, circuits) registers and counters
• Designing and creating a sequential system

Course title
Automatic

Objectives
At the end of this course, students will:
• acquire basic analytical skills and methods for automatic control engineering and the study of closed loops
• learn about the elementary functions of industrial control systems
• be familiar with the advantages of closed loop control
• be able to quantify the performance of closed-loop linear control systems
• be able to calculate the parameters of a PIC controller using various theories and experiments.

List of topics
• Industrial processes
• Open and closed loop control
• Performance of closed loop systems (accuracy, stability, rapidity)
• Elementary compensators: proportional, integral, derivative (P, I, and D), and
• Controllers (P, I, D)

Course title
Object Oriented Programming with Java

Objectives
At the end of this course, students will be able to:
• Write, test and set up a Java program and documentation from a given situation
• Use vocabulary relating to OO languages within the framework of Java
• Explain the design and set up for the life-cycle of a Java program / explain the design process and working of a Java program (what Bytecode is and the role of a JVM).
Course Outline & Guidelines
Master in Sciences and Technology | Embedded Electronic Systems

- Modify a class diagram (with 4 or 5 classes)
- Document code and create the Javadoc
- Respect Java writing code structures
- Use existing classes and packages
- Put into place exceptions handling
- Make modifications using Swing GUI
- Trigger ActionEvents
- Use basic Eclipse functions: editing, compiling, operating, importing and debugging

* This course will also help students to improve their team-work skills and their understanding of technical documents

List of topics
- Fundamental tools and techniques:
  - Storing information, communicating information, making choices, creating repetitions
- Initiation to Object-Oriented programming:
  - From algorithms to writing functions, classes and objects, UML classes
- More tools and techniques:
  - Collecting objects (a fixed amount and undetermined amount), using it with UML
  - Creating a graphical interface

Course title
C Programming

Objectives
At the end of this course, students will be able to write and develop a programme in C language, using:
- Functions: definitions, interests, prototypes
- 1 & 2 D arrays: syntax, use, parameters
- String functions: manipulating chains of characters
- Pointers: syntax, manipulation, using them correctly
- Structures: syntax, manipulation, establishing parameters
- Binary and text files: manipulation and relation to structures
- Dynamic allocation

List of topics
- Algorithms, processors, fundamentals, environment and variables
- Simplified architecture of a computer
- C Language: programming structure, declarations, control structures (if, switch, while, do while, for), entries / exits (printf, scanf, fflush role)
- Environment for development
- 1D arrays
- Review of general notions for arrays, functions, character chains, structures, pointers, dynamic allocation, files
Course title

Minor project

Objectives
At the end of this project, students will:

- familiarise themselves with a real-world situation similar to that of future professional environments
- acquire skills to exercise their initiative and independence
- improve their organizational, interpersonal and communication skills
- learn to manage time

List of topics
- Designing a product
- Product testing

Course title

Fundamentals of Electronics

Objectives
- At the end of this course, students will be able to:
  - Put together an electrical circuit in the form of a four-terminal network (transmit gain, input / output impedance)
  - Transcribe a situation into a simulation diagram
  - Choose the type of analysis (polarisation or time-frequency analysis)
  - Identify function block diagrams
  - Design a cabling schema from a given electric schema (using BNC connectors correctly)
  - Measure voltage using oscilloscopes, multimeters and dB meters
  - Create various wave forms, recognize them using an oscilloscope and change settings
  - Measure input/output impedance
  - Measure frequency response
  - Interpret results of the aforementioned measurements
  - Use Excel to plot graphs and schemas

List of topics
- Electrical circuits
- Simulation schema
- Block diagrams
- Cabling and electric schema
- Measurement
- Generation of various signals
- Generation of plot graphs
Course title

**English as a Foreign Language**

Objectives
At the end of this course, students will be able to:

Oral comprehension
- understand standard English used in everyday situations at work, school, etc.

Written comprehension
- understand texts written in standard English used in everyday situations such at work, school, etc.

Oral expression
- participate in a regular day-to-day conversation on familiar topics
- ask and exchange information
- prepare and give a short formal presentation

Written expression
- write short, clear and coherent texts on familiar/everyday situations with basic grammar and vocabulary

List of topics
- Revision of grammar and vocabulary

Assessment
Test of English for International Communication (TOEIC).

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Course title

**French as a Foreign Language**

Objectives
At the end of this course, students will be able to:

Oral comprehension
- understand standard English used in everyday situations at work, school, etc.

Written comprehension
- understand texts written in standard English used in everyday situations such at work, school, etc.

Oral expression
- participate in a regular day-to-day conversation on familiar topics
- ask and exchange information
- prepare and give a short formal presentation

Written expression
- write short, clear and coherent texts on familiar/everyday situations with basic grammar and vocabulary
Course title: Microprocessors

Objectives
At the end of this course, students will be able to:
- Understand the architecture of microprocessors
- Program microprocessors
- Study the evolution of their architecture

List of topics
- Microprocessor architecture (ALU, control unit, registers, buses)
- Data and processors (address decoding, synchronization)
- Vital signs of processors (clocks, power supply, reset)
- Microprocessor programming (languages, registers, addresses, instructions)
- Execution time, routines, passing parameters
- Principles and how exceptions/interruptions work
- Inputs/outputs
- Case study (MSP430)

Course title: VHDL and Logic Synthesis

Objectives
At the end of this course, students will be able to:
- Program logic devices (PLD)
- Develop programs using VHDL language

List of topics
- Review of combinatory and sequential logic
- The different families of programmable logic devices
- Practice with synthesis tools (Xilinx or Altera targets, Quartus or ISE tools, Modelsim)

Course title: Communication Buses

Objectives
At the end of this course, students will:
- Be able to use the most widely used communication buses in the field of embedded processors
- Understand technical specifications
Course title: **Real-time Operating Systems**

Objectives: At the end of this course, the students will be able to:
- Understand why real-time executive is used in embedded systems
- Describe the four major categories of services provided by an executive
- Describe the necessary required materials to implement an executive in real-time
- Learn the various commercial aspects of executive suppliers
- Describe the role of scheduling, how it works and the major variations
- Calculate task times for simple situations
- To be able to list attribution rules for task priority
- Describe how the principle elements for synchronization are presented in executives
- Describe the characteristics and how an email inbox works
- Design and develop a simple multitasking application with MicroC/OSII

List of topics:
- Fundamentals of multitasking and real-time
- A scheduler: its role and how it works
- Why real-time executives are used in embedded systems
- Necessary materials
- Categories of executives and their markets
- A real-time kernel: MicroC/OSII (Micro-Controller Operating Systems Version 2)
- Memory management
- Intertask communication and synchronization tools
- Using MicroC/OSII and microcontrollers

Course title: **Embedded Linux**

Objectives:
- Understand the possibilities and uses of the Linux kernel for an embedded IT project.
- Learn the principle software tools used in the Linux/Unix world and how to use them to develop.
- Be able to write a device driver for specific Linux run material
- Be able to combine tools to create advanced functions with a minimum of programming

Coursework:
- Introduction to Linux:
  - How an OS fits in an embedded system.
  - History of Linux and Unix systems.
  - Linux compared to other embedded operating systems.
Course title: **Embedded C Programming**

Objectives
At the end of this course, students will:
- Be familiar with the C coding practices for embedded systems
- Be familiar with the elements and tools for embedded software validation
- Develop, write and test a C language program (as per design specifications) to be used with a microprocessor from a modelling tool like SART
- Analyse and enumerate the various phases of development for a software project: the V cycle

List of topics
- Specificities of C Language for embedded systems (variables, memory organization, physical address access, etc.)
- Programming methods
- Software analysis and validation tools and principles for embedded systems

Course title: **Embedded Java**

Objectives
At the end of this course, students will:
- Be familiar with a computer language which can be used to develop graphic applications under Windows for personal embedded systems like Pocket PCs

List of topics
- Java ME environment: interface and syntax
- Basics of programming in the Java ME environment

Course title: **Visual Instrumentation**

Objective
At the end of this course, students will:
- Be familiar with the principles of virtual instrumentation through the use of LabVIEW software

List of topics
- Definition of virtual instrumentation compared with classical instrumentation
- Virtual instrumentation tools (hardware and software)
• Programming with LabVIEW software
• Advanced functions on LabVIEW (File management, Properties nodes, etc.)
• Network functions on LabVIEW (Datasockets, TCP, UDP, etc.)
• NI-Vision Toolkit
• Practice with real sensors

Course title
Specific Instrumentation

Objective
At the end of this course, students will be able to:
• Manage the entire information sampling chain in an instrumentation-type embedded system

List of topics
• The measurement chain: physical signal to digital processing
• Sensors: types, technology
• Signal conditioning: transport, filtering, amplification
• Sampling: period, response time
• Information security: accuracy, lifetime, redundancy

Course title
MtoM Communication

Objectives
At the end of this course, students will be able to:
• Be familiar with the principles of communication between machines, needing no human action

List of topics
• Sensors and servers
• Cellular networks
• Applications
• Protocols of MtoM communication

Course title
Smart Sensors

Objectives
At the end of this course, students will be able to:
• Be familiar with the principles and the advantages of smart sensors through different applications

List of topics
• Sensors and interfacing circuits
• Applications of smart sensors
• Architecture and components of smart sensors
• Practice with smart sensors
Course title

System on Chip

Objectives
At the end of this course, students will:

• Understand and be able to implement a complete embedded system on a chip (SoC)

List of topics

• Main components of SoC systems
• Related embedded solutions on chips
• Defining an intellectual property tool
• Integration of a solution
• Xilinx Spartan component

Course title

DSP Processors

Objectives
At the end of this course, students will:

• Be familiar with the main DSP (digital signal processing) algorithms and their impact on DSP architecture

List of topics

• Sampling, convolution
• Linear filtering
• Fourier transforms
• TMS320C6xxx architecture

Course title

Safety Systems

Objectives
At the end of this course, students will:

• Understand the role EMC phenomena play in the field of embedded systems, by studying automotive examples

List of topics

• EMC (Electromagnetic Compatibility) issues for electronics
• Cause and effect
• Prevention and solutions
• The automotive field: an overview
Course title
Cross Cultural Awareness/ Teamworking

Objectives
At the end of the module students will be able to:
• Understand the changing views and theories of leadership in history.
• Understand the dynamics and roles of people in teams.
• Understand the impact of different cultures on management styles.
• Apply leadership theory in all aspects of life.
• Use a range of tools / aide-mémoires to facilitate good leadership.

The ability to demonstrate leadership is an important aspect of human development in general and in the employability of Master’s students. This module will focus on:
• The theories of leadership and their practical application, together with practical tools for the graduate manager.
• The application and analysis of leadership theories in the classroom.
• A short “business game” to illustrate the challenges of leadership in a hierarchical environment.
• The task and human factors of team membership and leadership through the use of the Belbin Team Styles instrument.

Coursework
The course includes:
• Leadership in history and its relation to cultural norms.
• Modern leadership models and their application.
• Maslow’s hierarchy of needs and its role in management.
• The J Adair model and its use in work and in the student environment.
• Belbin team roles, student participation in the “test”. The use of Belbin roles in student and work situations.
• The need for communication in leadership – business game to illustrate the difficulties of leadership.
• The influence of national cultures on leadership.
• The building and management of international, multi-discipline, remote and virtual teams.

Course title
Oral Communication

Objectives
Students will be able to practice their use of the English language in the context of oral presentations which they will be required to produce, for instance, at the end of the integration project and for the professional thesis.

Coursework
The course includes:
• Methods used to prepare an oral presentation.
• Simulations
Course title

Project Management

Objectives
At the end of the module, students will be able to:

- Appreciate the need for project management as a recognised discipline
- Understand the complexity of IT projects and the need for formal methods
- Appreciate the need to break up complex projects
- Appreciate the need for effective planning, monitoring and control mechanisms
- Understand the need for formal project management organisational structures
- Understand the importance and management of stakeholders in an international project
- Construct a project timeline and resource schedule using MS Project
- Use MS Project as a planning, controlling and reporting tool
- Understand the complexities and risks introduced by international and cross-organisational project teams
- Use formal leadership techniques to manage projects and project teams

Course title

Engineering Project

Objectives
Students will be able to:

- Exercise their initiative and independence.
- Improve their organizational skills (within a team, facing deadlines) and manage their time.
- Improve their communication skills.
- Work in a real-world situation close to their future professional environments.

Coursework
The project includes the following stages:

- Constitution of the group.
- Technical / feasibility studies.
- Developing functional specifications and success strategies.
- Development.
- Test.

Remark- The programme can be modified in function of teacher’s prerogatives or organizational constraints.
**Internship / professional thesis**

The internship will take place either in a company or in a research laboratory in a university. Students are encouraged to do their internship in France / Europe but may choose to do so elsewhere in the world too. The duration of the internship is of 4 (min.) to 6 months (max.). ESIGELEC provides assistance to students to find internships but they are expected to play an active part, as the internships are not handed out automatically. A professional thesis will have to be submitted upon completion of the internship and the students will have to make an oral presentation before a convened jury, at ESIGELEC (or remotely, upon special written request, authorised by the school).

An internship form, providing all required information must be filled and submitted to the Internship Department at ESIGELEC, as soon as the student has obtained an offer. The Head of the Internship Department and the Academic Coordinator of the Master’s Programme will validate and approve the information (if relevant) by duly signing on the said form. ESIGELEC, the company / research laboratory and the student will then countersign an Internship Agreement issued at ESIGELEC. A copy of the agreement is retained by ESIGELEC, the company / research laboratory and the student.

A faculty member will be assigned the task of visiting/contacting the student at least once during the internship. In the event of questions regarding the internship, the preparation of the oral presentation and/or the professional thesis, the student may remain in contact either with the assigned faculty member or the Academic Coordinator of the Master’s Programme, during the period of the internship or thereafter.

The topic of the professional thesis chosen by the student must be communicated to the Academic Coordinator of the Master’s Programme for approval, within the first month of starting the internship.

The professional thesis must be submitted to ESIGELEC one month, at the latest, after completion of the internship. The oral presentation must be made before a Jury comprising of a President (from ESIGELEC or outside), one faculty member from ESIGELEC and the industrial tutor (if possible) two months, at the latest, after completion of the internship. The total duration of the oral presentation will be of 60 minutes (30 min. presentation + 15 min. Q&A + 15 deliberation among jury members).

A student has a maximum period of 2 years after the final academic semester, to find the internship, complete it, submit the professional thesis and conduct the oral presentation before a convened jury at ESIGELEC.

**The Study Board**

The Board of Studies of ESIGELEC, whose members are representatives from industry, universities & ESIGELEC, oversees the course content and recommends changes when necessary.

The Board of Studies, which meets at least once a year, also ensures that the course content and laboratories are streamlined in keeping with the changing industry requirements. A meeting between the Academic Coordinator of the Master’s Programme and all faculty members is convened at the end of each module, to assess the relevance of the content, equipment and issues which may have occurred while delivering the module.

A meeting is also convened every two months between the Academic Coordinator of the Master’s Programme and the students to discuss academic and non-academic issues.